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SECTION 14

SIGMA-DELTA ADCs AND DACs
Walt Kester, James Bryant

SIGMA-DELTA OVERVIEW

Within the last several years, the sigma-delta architecture for realizing high-resolution ADCs has become available in mixed-signal VLSI processes. Until recently, however, the process technology needed to make these devices commercially viable has not been available. Now that 1 micron and smaller CMOS geometries are manufactureable, sigma-delta converters will become even more prolific in certain types of applications, especially mixed-signal ICs which combine the ADC, DAC, and DSP functions on a single chip.

Conceptually, the sigma-delta architecture is more digital than analog intensive. This does not, however, minimize the importance of the analog portion of the sigma-delta ADC. The analog design of a fifth-order sigma-delta modulator (as in the AD1879 dual 18 bit ADC) is certainly not a trivial matter. The sigma-delta converter is inher-
ently an oversampling converter, although oversampling is just one of the techniques contributing to the overall performance. Basically, a sigma-delta converter digitizes an analog signal with a very low resolution (1 bit) ADC at a very high sampling rate. By using oversampling techniques in conjunction with noise shaping and digital filtering, the effective resolution is increased. Decimation is then used to reduce the effective sampling rate at the ADC output. The sigma-delta ADC exhibits excellent differential and integral linearity due to the linearity of the 1 bit quantizer and DAC, and no trimming is required (unlike other ADC architectures).

The key concepts involved in understanding the operation of sigma-delta converters are *oversampling, noise shaping* (using a sigma-delta modulator), *digital filtering*, and *decimation*.

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SIGMA-DELTA CONCEPTS

- ■ Ideal Topology for Mixed Signal VLSI Chips

- ■ Oversampling

- ■ Noise-Spectrum Shaping Using Sigma-Delta Modulator

- ■ Digital Filtering

- ■ Decimation

- ■ 16 Bits and Higher Resolution Possible Using One-Bit Quantizer

Figure 14.1

OVERSAMPLING

A major advantage of oversampling an analog signal is the resulting simplification in the analog antialiasing filter requirements. The disadvantage of simple oversampling is that it also increases the ADC output data rate which increases the required size of the buffer memory; and in real-time DSP applications, there is less time between samples to perform calculations. An attractive alternative to simple oversampling makes use of both analog *and* digital filtering techniques and a process called *decimation* (Figure 14.2).

The top portion of the figure shows the case of traditional Nyquist sampling. In the lower portion of the diagram, the sampling rate has been increased by a factor of K (the oversampling ratio). Note the resulting relaxation of the requirement on the analog antialiasing filter. The analog signal is sampled at

rate equal to Kf_s, and the new Nyquist bandwidth is $Kf_s/2$. Although the filter requirement is relaxed, the ADC output data rate is correspondingly higher.

If we apply the ADC data to a digital filter (as shown in the bottom portion of Figure 14.2), the energy falling between $f_s - f_a$ and Kf_s can be removed. Digital filters having sharp cutoff characteristics with good phase response are much more easily implemented than their corresponding analog counterparts (assuming sufficient speed in the DSP). Finite Impulse Response (FIR) filters can easily be designed with linear phase characteristics. Since the bandwidth has been reduced to $f_s/2$ by the digital antialiasing filter, the data coming out of the digital filter actually contains redundant information, and there is no need to use every sample. In fact, it is only necessary to look at every Kth

sample. This process is called *decimation*. The actual decimation can be performed by the FIR filter itself by computing a single output sample for every K input samples. Figure 14.3 illustrates the differences in traditional Nyquist sampling and oversampling with digital filtering.

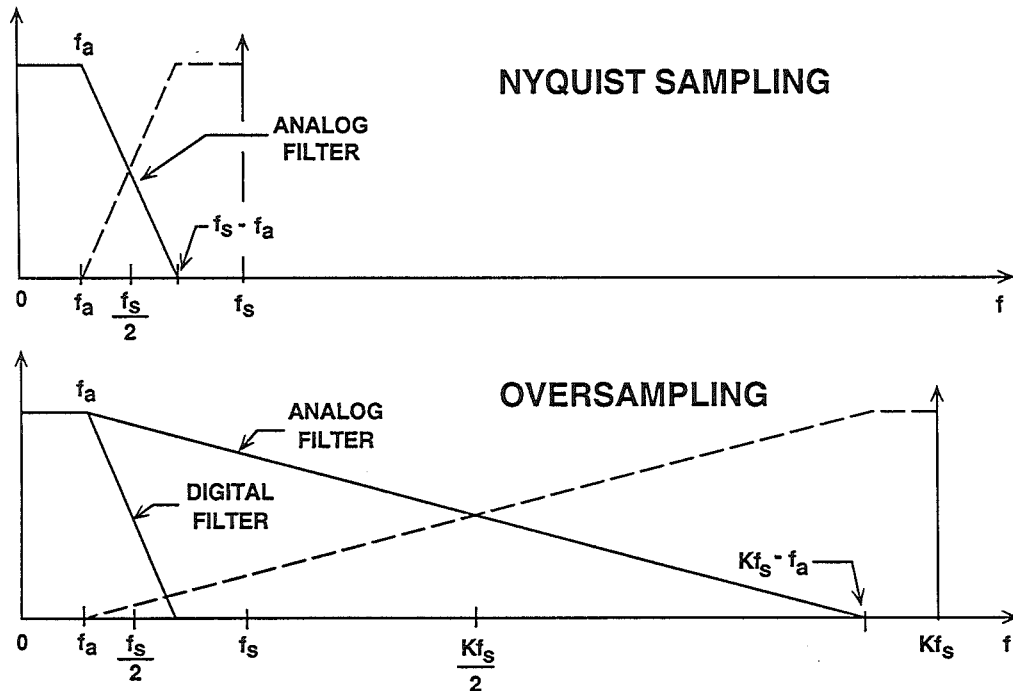## EFFECT OF OVERSAMPLING ON ANTIALIASING FILTER REQUIREMENTS

Figure 14.2

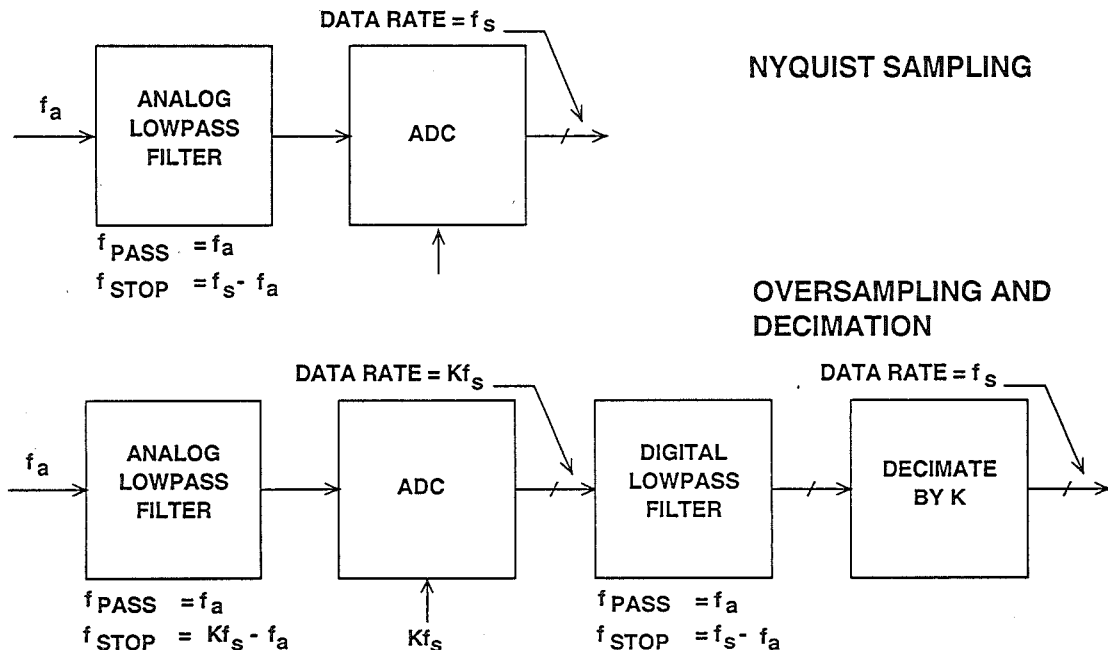## NYQUIST SAMPLING VERSUS OVERSAMPLING SYSTEMS

Figure 14.3

As discussed above, one significant benefit of oversampling is that the rolloff requirements on the analog antialiasing filter are relaxed. There is an additional benefit which relates to the quantization noise spectrum and the ADC dynamic range. The theoretical quantization noise has an rms value of $q/\sqrt{12}$, where q is the weight of the LSB. In Nyquist sampling, this noise is spread uniformly over the bandwidth dc to $f_S/2$ as shown in the top portion of Figure 14.4. If the sampling rate is increased by a factor of K (the oversampling ratio), the rms value of

the quantization noise remains the same, but it is now spread out over a bandwidth dc to $Kf_S/2$ (see the bottom portion of Figure 14.4). The noise which falls between $f_S/2$ and $Kf_S/2$ is removed by the digital filter (K is the oversampling ratio). This has the effect of increasing the overall signal-to-noise ratio by an amount equal to $10\log_{10}(K)$. Unfortunately this is a high price to pay for extra resolution, as an oversampling ratio of 4 is required just to increase the signal-to-noise ratio by a modest 6dB (1 bit).
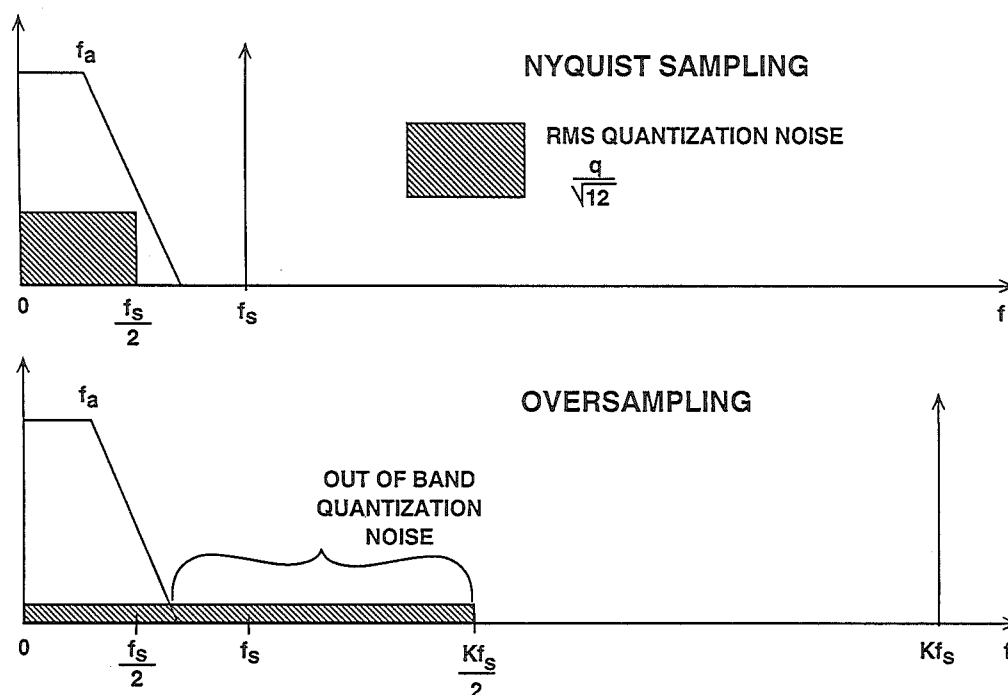
EFFECT OF OVERSAMPLING ON QUANTIZATION NOISE

Figure 14.4

To keep the oversampling ratio within reasonable bounds, it is possible to shape the frequency spectrum of the quantization noise so that the majority of the noise lies between $f_S/2$ and $Kf_S/2$, and only a small portion is left between dc and $f_S/2$. This is precisely what a sigma-delta modulator does in a sigma-delta ADC. After the noise spectrum is

shaped by the modulator, the digital filter can then remove the bulk of the quantization noise energy, and the overall signal-to-noise ratio (hence the dynamic range) is dramatically increased. This allows a single-bit ADC (comparator) to provide high resolution and dynamic range with a reasonable oversampling ratio.

SIGMA-DELTA MODULATORS AND QUANTIZATION NOISE SHAPING

A block diagram of a first-order sigma-delta ADC is shown in Figure 14.5. The first part of the converter is the sigma-delta modulator which converts the input signal into a continuous serial stream of 1's and 0's at a rate determined by the sampling clock frequency, Kf_s. The 1-bit DAC is driven by the serial output data stream, and the DAC output is subtracted from the input signal. Feedback control theory tells us that the average value of the DAC output (hence the serial bit stream) must approach that of the input signal if the loop has enough gain. The integrator can be represented in the frequency domain by a filter whose amplitude response is proportional to 1/f, where f is the input frequency. Since the chopper-like action of the clocked, latched comparator converts the input signal to a high-frequency ac signal, varying about the average value of the input, the effective quantization noise at low frequencies is greatly reduced (the integrator looks like a high-pass filter to quantization noise). The exact frequency spectrum of the resulting noise depends on the sampling rate, the integrator time constant, and the precise span of the voltage fed back.
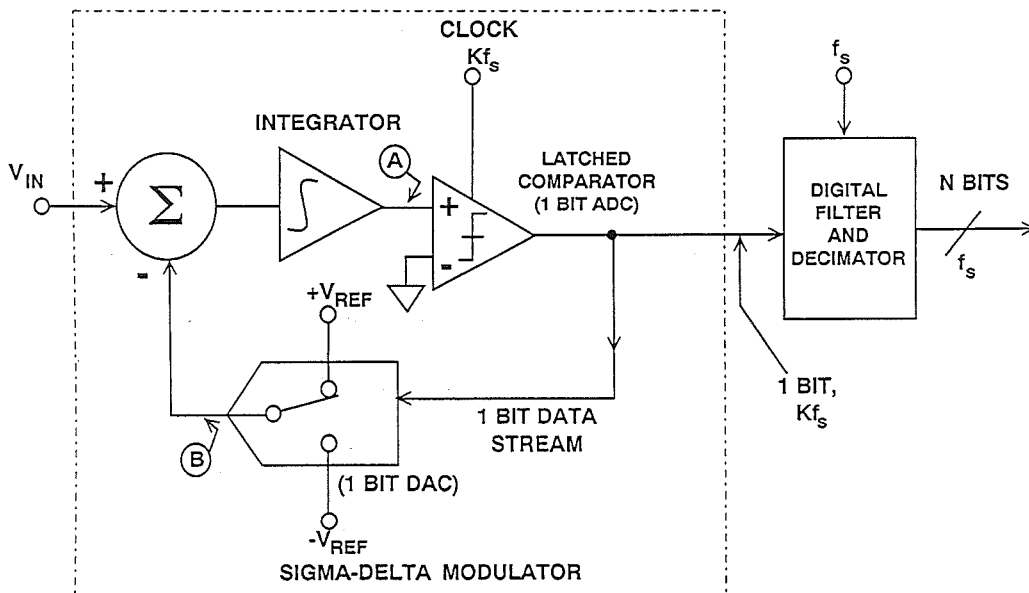
FIRST-ORDER SIGMA-DELTA ADC

Figure 14.5

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For any given input value in a single sampling interval, the data from the 1-bit ADC is meaningless. Only when a large number of samples is averaged will a meaningful value result. The sigma-delta modulator is difficult to analyze in the time domain because of this apparent randomness of the single-bit data output. If the input signal is near positive fullscale, it is clear that there will be more 1's than 0's in the bit stream. Likewise, for signals near negative fullscale, there will be more 0's than 1's in the bit stream. For signals near midscale, there will be approximately equal numbers of 1's and 0's. Figure 14.6 shows the output of the integrator for two input conditions. The first is for an input of zero (midscale). To decode the output, pass the output samples through a simple digital lowpass filter that averages every four samples. The output of the filter is 2/4. This value represents bipolar zero. If more samples are averaged, more dynamic range is achieved. For example, averaging 4 samples gives 2 bits of resolution, while averaging 8 samples yields 4/8, or 3 bits of resolution. In the bottom waveform of Figure 14.6, the average obtained for 4 samples is 3/4, and the average for 8 samples is 6/8.
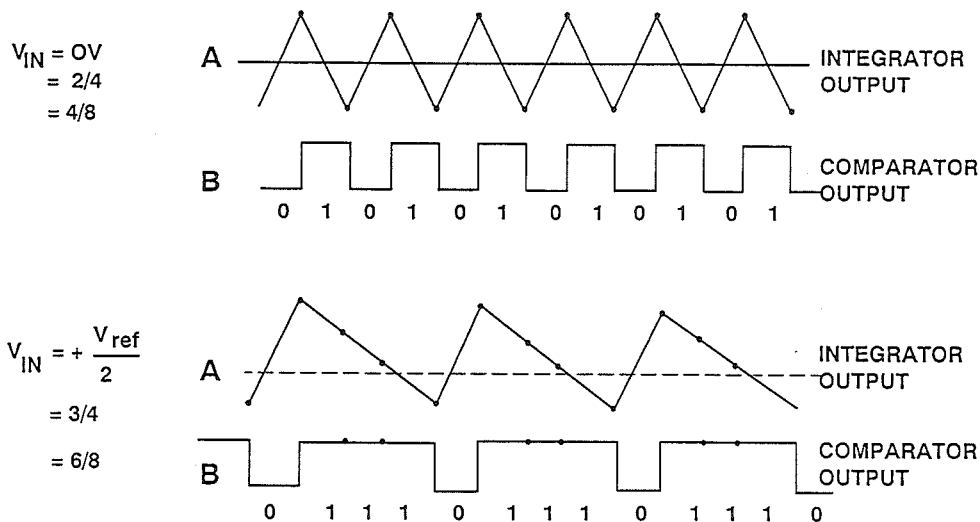
SIGMA-DELTA MOLULATOR WAVEFORMS

Figure 14.6

But the sigma-delta ADC cannot just be viewed as a synchronous voltage-to-frequency converter followed by a counter. True, if the number of 1's in the output data stream is counted over a sufficient number of samples, the counter output will represent the digital value of the input. But a simple VFC followed by a counter must double its sampling interval for each bit's increase in resolution (i.e. a 20-bit ADC using such an architecture must sample for at least a million clock cycles). The value of the ΣΔ ADC is that it requires a much lower over-sampling ratio. while the purpose of this seminar is to show *what* happens, rather than give a detailed description of *why* it happens, a brief description of the operation of a ΣΔ ADC in the frequency domain is appropriate at this point. Consider the linear model in Figure 14.7.

FREQUENCY DOMAIN LINEARIZED MODEL
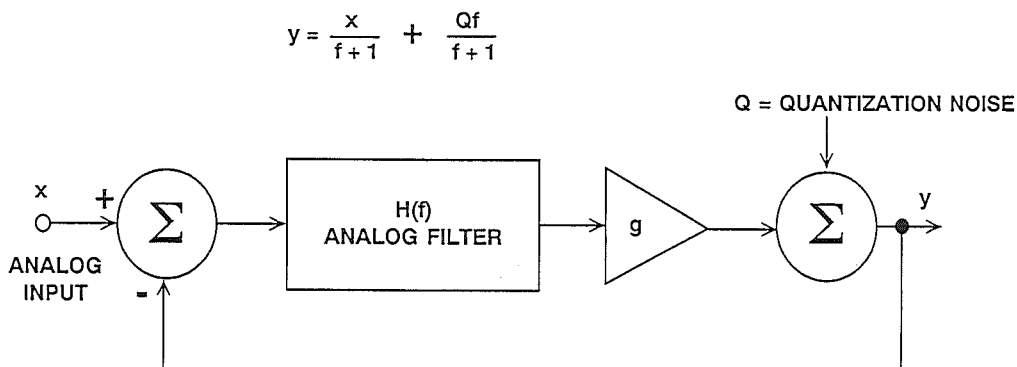# OF A SIGMA-DELTA MODULATOR

$$y = \frac{x}{f+1} + \frac{Qf}{f+1}$$

Q = QUANTIZATION NOISE

Figure 14.7

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The integrator is represented as an analog filter with a transfer function H(f). This transfer function has an amplitude response which is inversely proportional to the input frequency. The quantizer is modeled as a gain stage and is followed by the addition of quantization noise. If we set the gain to 1, and the transfer function is represented as 1/f, the following mathematical relationship results:

$$y = \frac{x - y}{f} + Q \text{ , or by rearranging,}$$

$$y = \frac{x}{f+1} + \frac{Qf}{f+1}.$$

Note that as frequency f approaches zero, the output approaches x with no noise component. At higher frequencies, the value of x is reduced, and the value of the noise component is increased. At high frequency, the output consists primarily of quantization noise. In essence, the analog filter has a low pass effect on the signal and a high pass effect on the quantization noise. The analog filter of the modulator can thus be viewed as a noise shaping filter (Figure 14.8).

With analog filters in general, higher order filters offer better performance. This is also true of the sigma-delta modulator, provided certain precautions are taken. A second order sigma-delta modulator is shown in Figure 14.9, and a comparison between the noise shaping functions is shown in Figure 14.10. Figure 14.11 shows a plot of the in-band signal-to-noise ratio (dynamic range) as a function of the oversampling ratio for first, second, and third order modulators. Note that the first order transfer function has a slope of 9dB per octave, while each succeeding increase in order yields an additional 6dB/octave. Loops of third order or greater, although yielding even lower oversampling ratios, are potentially unstable, and must be designed with great care. Fortunately there is so much computation inherent in an FIR filter that it is generally possible to use spare resources in the "computer" in the FIR filter to recognize the onset of instability and take steps to damp it - but the design of such a system may not be a trivial task.
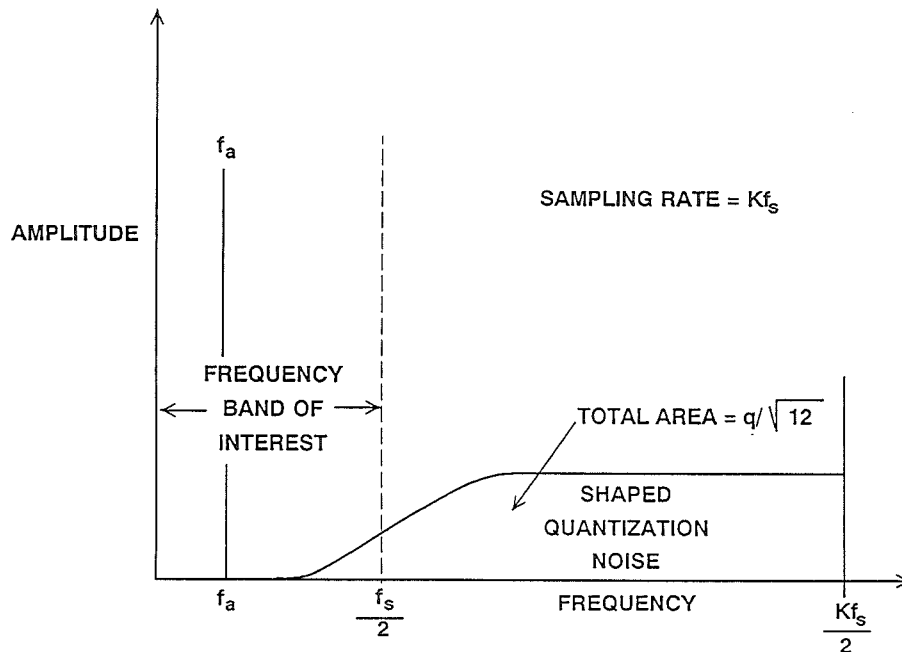
SHAPED QUANTIZATION NOISE DISTRIBUTION
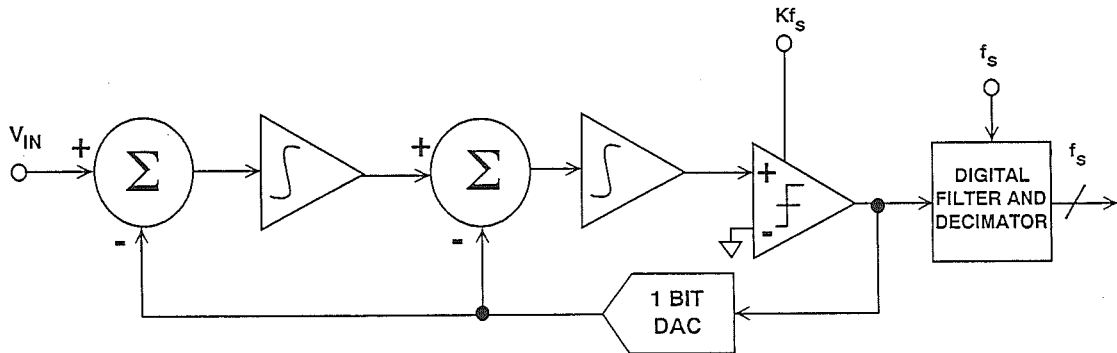

Figure 14.8

SECOND-ORDER SIGMA-DELTA MODULATOR

Figure 14.9

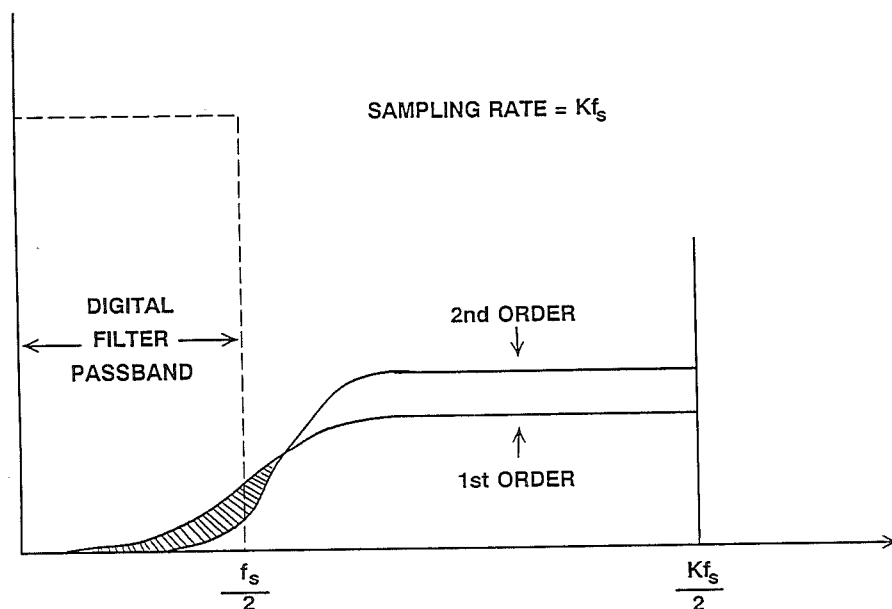# FIRST AND SECOND-ORDER NOISE SHAPING FUNCTIONS

Figure 14.10

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SNR VERSUS OVERSAMPLING RATIO
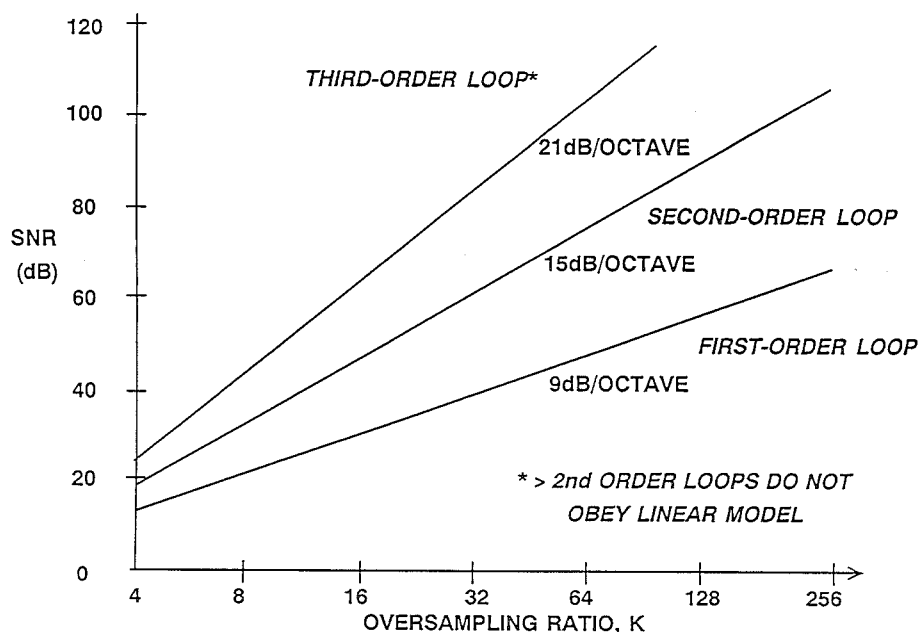## FOR FIRST, SECOND, AND THIRD-ORDER LOOPS

Figure 14.11

The curves in Figure 14.11 can be used to determine the approximate ADC resolution, given the modulator order and the oversampling ratio. For instance, if the oversampling ratio is 64x, an ideal second order system is capable of providing a signal to noise ratio of about 80dB. This implies an ADC resolution of approximately 13 bits. Although the filtering done by the digital filter can be done to any degree of precision desirable, it would be pointless to carry more than 13 binary bits to the outside world. Additional bits would carry no useful signal information, and would be buried in noise.

DIGITAL FILTERING AND DECIMATION

After the quantization noise has been shaped by the modulator and so that it occurs mainly at frequencies above the band of interest, digital filtering can be applied to this shaped quantization noise as (Figure 14.12). The purpose of the digital filter is twofold. First, it acts as an antialiasing filter with respect to the final sampling rate, f_S. Second, it filters out the high frequency noise produced by the noise-shaping process of the sigma-delta modulator.

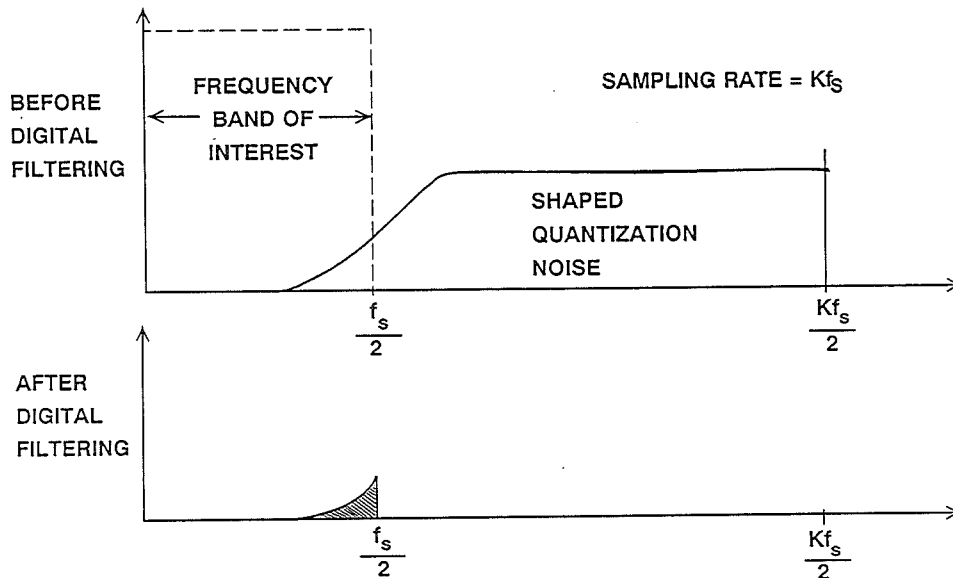# EFFECTS OF DIGITAL FILTERING
ON SHAPED QUANTIZATION NOISE

Figure 14.12
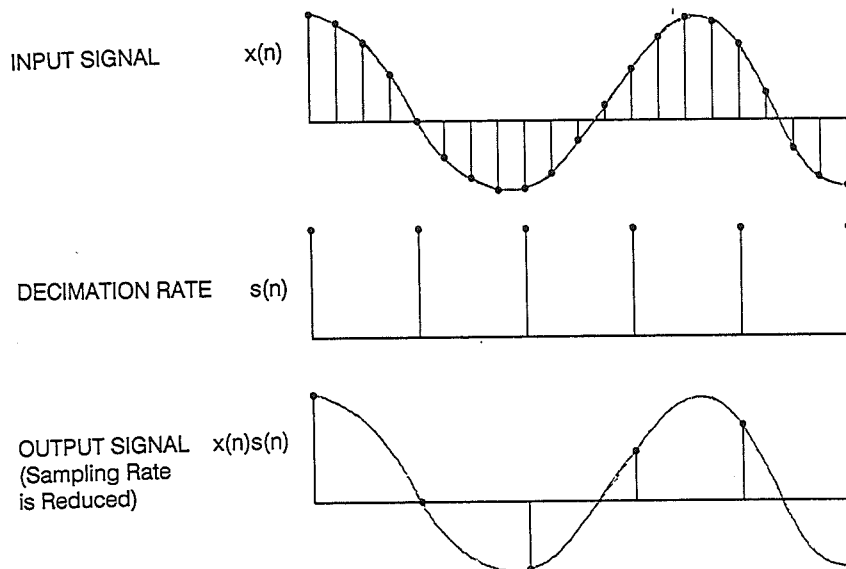
DECIMATION OF A DISCRETE-TIME SIGNAL

Figure 14.13

The final data rate reduction is performed by resampling the filtered output using a process called decimation. The decimation of a discrete-time signal is shown in Figure 14.13, where the sampling rate of the input signal x(n) is at a rate which is to be reduced by a factor of 4. The signal is resampled at the lower rate (the decimation rate), s(n). Decimation can also be viewed as the method by which the redundant signal information introduced by the oversampling process is removed.

In sigma-delta ADCs it is quite common to combine decimation with digital filtering. This results in an increase in computational efficiency.

Recall that a finite impulse filter (FIR) simply computes a moving weighted average (the weighting being determined by the individual filter coefficients) of the input samples. Normally, there is one filter output for every input sample. If, however, we wish to decimate the filter output by digitally resampling at a lower rate, it is no longer necessary to compute a filter output for every input sample. Instead, we only compute filter outputs at the lower decimation rate, thereby improving the efficiency of the computation.

An IIR filter, like many analog active filters, uses feedback. The result of each computation is used in later computations, and all intermediate results are used. It is therefore impossible to perform decimation as part of the filtering process in an IIR filter. In some sigma-delta ADC designs, the filtering is performed in two stages. If both FIR and IIR filters are used, the decimation is performed in the first FIR stage, and the final filtering is done in the later IIR stage. If FIR filters are used for both stages, it is usually more efficient to split the decimation between the two stages.

From the above discussion it should be clear that the design of a sigma-delta ADC digital filter involves many tradeoffs. FIR filters lend themselves to decimation, are always stable, and have linear phase characteristics (extremely important in audio and some telemetry applications). Although they are easier to design, they generally require more stages to realize a given transfer characteristic than an IIR filter. On the other hand, the IIR filter employs feedback which eliminates the possibility of decimation within the filter, but makes the filter more efficient (better filter performance with fewer calculations). The feedback used in IIR filters can lead to instability, and also may require the use of higher resolution digital processors to avoid overflow during computation. IIR filters often exhibit nonlinear phase response, and their design procedures are more complex than those of FIR filters.

SIGMA-DELTA ADC DIGITAL FILTERING AND DECIMATION

FIR Filters: ■ Easy to Design
■ Easy to Incorporate Decimation
■ Linear Phase Response
■ Large Number of Coefficients May Be Required

IIR Filters: ■ Stability, Overflow Considerations
■ Cannot Decimate Internally Due to Feedback
■ More Efficient than FIR Filters
■ Non-Linear Phase Response

Combinations: ■ 2-Stage FIR Filters
■ FIR Filter Followed by IIR Filter
■ 2-Stage IIR Filters

Figure 14.14

IDLE TONES IN SIGMA-DELTA ADCs

In our discussion of sigma-delta ADCs up to this point, we have made the assumption that the quantization noise produced by the sigma-delta modulator is random and uncorrelated with the input signal. Unfortunately, this is not entirely the case, especially for the low-order modulators. Consider the case where we are averaging 16 samples of the modulator output in a 4 bit sigma-delta ADC. Figure 14.15 shows the bit pattern for two input signal conditions: an input signal having the value 8/16, and an input signal having the value 9/16. In the case of the 9/16 signal, the modulator output bit pattern has an extra "1" every 16th output. This will produce energy at $f_s/16$, which translates into an unwanted tone which is known as an *idle* tone. If the oversampling ratio is less than 16, this tone will fall into the passband. Figure 14.16 shows the correlated idling pattern behavior for a first order sigma-delta modulator, and Figure 14.17 shows the less correlated pattern for a second-order modulator. The higher the order of a $\Sigma\Delta$ ADC the less the problem of idle tones, although even the highest order devices are not always entirely free of them. For this reason, and because of their relatively poor (i.e. large) oversampling ratio, first order $\Sigma\Delta$ ADCs are not often used.

14

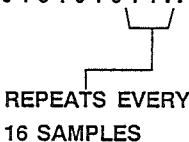# REPETITIVE BIT PATTERN IN SIGMA-DELTA MODULATOR OUTPUT

16 SAMPLES OF SIGMA-DELTA MODULATOR DATA OUTPUT STREAM		BINARY EQUIVALENT
1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 ... 8/16	=	1000
1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 1 ... 9/16	=	1001

REPEATS EVERY
16 SAMPLES

Figure 14.15

IDLING PATTERNS FOR FIRST-ORDER SIGMA-DELTA MODULATOR (INTEGRATOR OUTPUT)

IDLE BEHAVIOR WITH 0 VOLTS INPUT

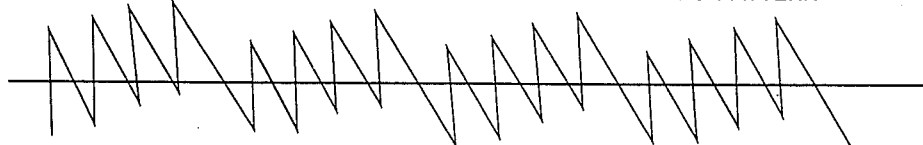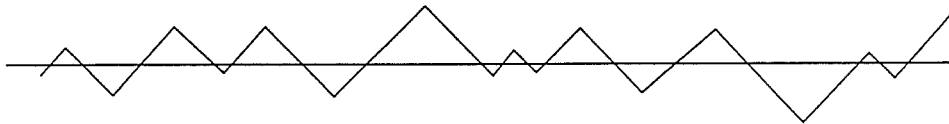IDLE BEHAVIOR WITH DC INPUT SHOWING CORRELATED IDLING PATTERN

Figure 14.16

IDLING PATTERNS FOR SECOND-ORDER SIGMA-DELTA MODULATOR (SECOND INTEGRATOR OUTPUT)

IDLE BEHAVIOR WITH 0 VOLTS INPUT

IDLE BEHAVIOR WITH DC INPUT

Figure 14.17

Hɪɢʜᴇʀ Oʀᴅᴇʀ Mᴏᴅᴜʟᴀᴛᴏʀ Lᴏᴏᴘs

In order to achieve wide dynamic range, sigma-delta modulator loops greater than second-order are necessary, but present real design challenges. First of all, the simple linear models previously discussed are no longer fully accurate. Loops of order greater than two are generally not unconditionally stable under all input conditions. The instability arises because the comparator is a non-linear element whose effective "gain" varies inversely with the input level. This mechanism for instability causes the following behavior: if the loop is operating normally, and a large signal is applied to the input that overloads the loop, the average gain of the comparator is reduced. The reduction in comparator gain causes loop instability, which persists even when the signal that caused it is removed. In practice, such a circuit would normally oscillate on power-up due to turn-on transients.

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HIGHER ORDER LOOP CONSIDERATIONS (>2)

■ Increased Dynamic Range and Resolution is Achievable

■ Higher Order Loops Minimize Idling Patterns and Tones

■ Difficult to Analyze and Stabilize

■ Non-Linear Stabilization Techniques Can Be Used
   Successfully: AD1879 18 Bit, 5th Order ADC

Figure 14.18

Instability in the AD1879 fifth-order modulator is sensed by counting the number of consecutive ones or zeros in the modulator bit stream. A sufficiently long string of either ones or zeros indicates modulator instability. This triggers circuitry which resets the integrators to restore stability.

DESCRIPTION OF THE AD776 THIRD-ORDER SIGMA-DELTA ADC

The AD776 is a general purpose 16 bit, 100kSPS sigma-delta ADC designed for DSP applications. A block diagram is shown in Figure 14.19 and key specifications are summarized in Figure 14.20.

In the AD776, the output of the one-bit quantizer (6.4MHz data rate) is first passed through a 16-tap comb filter whose output is decimated by a factor of 16. The comb filter is a simple moving average filter and has the response shown in Figure 14.21. In the 400kSPS mode, the output of the comb filter provides the conversion data. In this mode, the dynamic range is equivalent to approximately 72dB, or 12 bits.

AD776 SIGMA-DELTA ADC GIVES 16-BIT, 100kSPS OUTPUT FROM FIR FILTER AND 12-BIT, 400kSPS OUTPUT FROM COMB FILTER

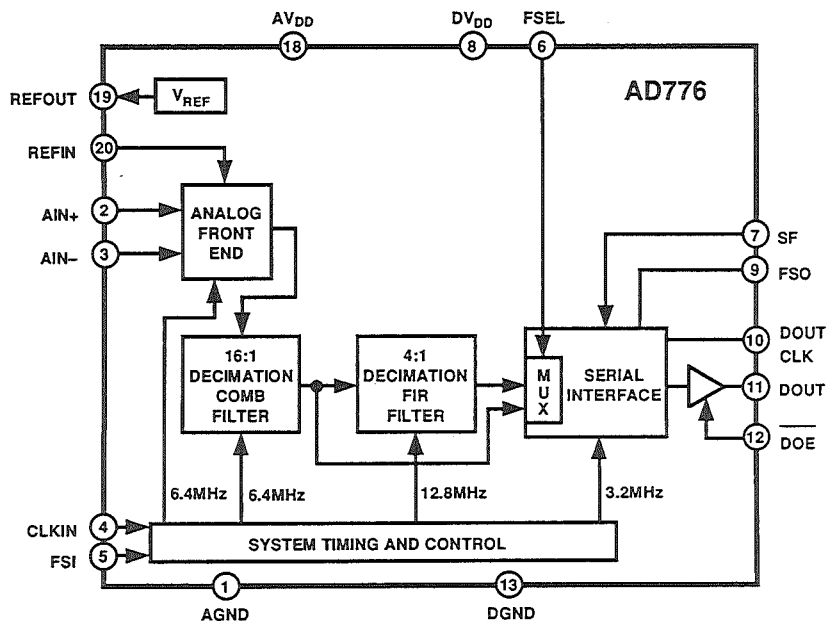

Figure 14.19

AD776 SIGMA-DELTA ADC KEY SPECIFICATIONS

■ 16 Bits @ 100kSPS or 12 Bits @ 400kSPS Output Rates

■ 64X Oversampling

■ Third-Order Noise Shaping

■ 90dB SNR, −100dBc Distortion For Up To 45kHz Inputs

■ Single +5V Supply, 350mW Power Dissipation

Figure 14.20

In the 16 bit, 100kSPS mode, the comb filter serves as the input to the 255-tap FIR filter. The FIR filter compensates for the passband roll-off of the comb filter and provides the final sharp cutoff required to remove the out-of-band quantization noise. Characteristics of the output of the FIR filter are also shown in Figure 14.21. The FIR filter has a 9% transition band, and with an input sampling rate of 6.4MSPS has a

45.5kHz passband cutoff frequency, 50kHz stopband frequency, 0.003dB passband ripple, and a stopband attenuation of 96dB. The FIR filter decimates the comb filter data rate by a factor of 4, thereby reducing the final output data rate to 100kSPS. The passband and stopband frequencies of both the comb and FIR filters scale linearly with the input sampling frequency.

AD776 DIGITAL FILTER RESPONSE CHARACTERISTICS FOR AN INPUT SAMPLING RATE OF 6.4MSPS

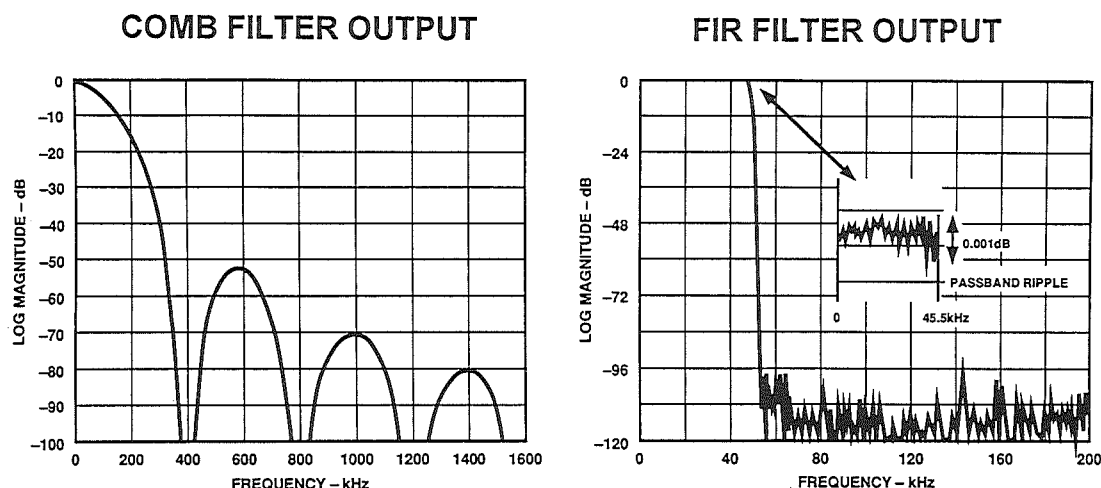### COMB FILTER OUTPUT

FIR FILTER OUTPUT

Figure 14.21

The internal digital filters in sigma-delta ADCs often limit their usefulness in applications requiring a multiplexed analog input. Figure 14.22 shows measured group delay and the settling time of the AD776 comb filter and FIR filter outputs. When a multiplexer switches between adjacent channels, it may present a fullscale step-function input to the ADC. For the AD776 FIR filter output, $680\mu s$ is required for the ADC to settle from a step-function input. This limits the maximum switch-

ing rate of the multiplexer to $1/680\mu s = 1.47kHz$ (neglecting the settling time of the multiplexer itself).

For data acquisition systems using analog multiplexers in front of the ADC, faster switching speeds can be obtained using non-sigma-delta ADCs with wide bandwidth front ends such as the AD7884/AD7885, or the AD676/AD677. These converters use traditional architectures, and their settling time is not limited by a built-in digital filter.

AD776 SIGMA-DELTA ADC DIGITAL FILTER GROUP DELAY AND SETTLING TIME CHARACTERISTICS

	Group Delay	Settling Time
Comb Filter Output	13.5µs	17µs
FIR Filter Output	340µs	680µs

Figure 14.22

The AD776 analog front-end sigma-delta modulators use a switched-capacitor architecture on both the signal and the reference inputs. In order to understand the implications on the input drive circuits, Figure 14.23 shows the basic circuit for a single-ended switched capacitor integrator. The capacitor is switched at the oversampling frequency, f_S, and acts as a resistor having a resistance equal to $1/Cf_S$. The integrator time constant is therefore determined by capacitance *ratios* which can be accurately controlled in a CMOS process. The resistance value is inversely proportional to the oversampling frequency. The switched capacitor is implemented in CMOS using the T-switch circuit shown in Figure 14.24. Because the input signal to the switch modulates the FET bias voltages, the charge injected into the drive amplifier (external to the ADC) is signal-dependent.
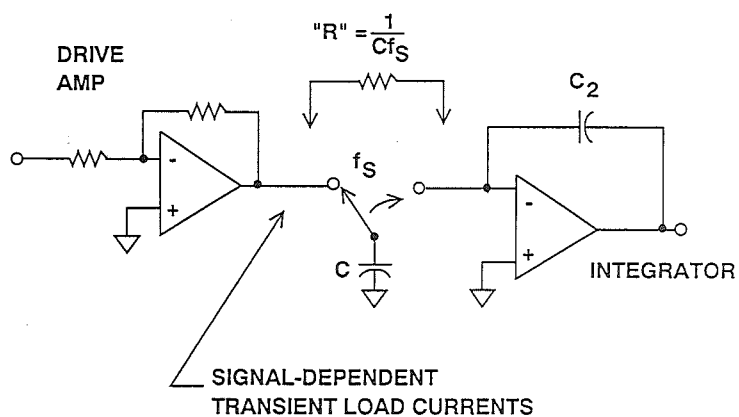
14

SINGLE-ENDED SWITCHED CAPACITOR INTEGRATOR

$$"R" = \frac{1}{Cf_S}$$

DRIVE
AMP

C_2

f_S

C

INTEGRATOR

SIGNAL-DEPENDENT
TRANSIENT LOAD CURRENTS

Figure 14.23

CMOS IMPLEMENTATION OF SWITCHED CAPACITOR

ϕ_1

ϕ_2

C_P

C_P

C

ϕ_1

$\leftarrow T \rightarrow$
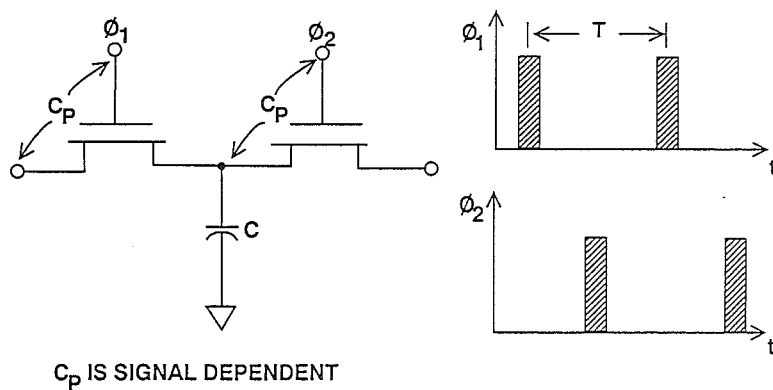
t

ϕ_2

t

C_P IS SIGNAL DEPENDENT

Figure 14.24

Care must therefore be taken in driving both the Analog Input of the AD776 and the Reference Input. Best performance is obtained when the Analog Input of the AD776 is driven differentially (Figure 14.25). The AD712 op amp has low distortion as well as fast settling time and low output impedance at high frequencies. The fast settling time and low output impedance is required because of the charge injection due to the switched capacitors. The nominal input voltage range of the AD776 is ±0.875V (differential) centered around a common-mode voltage of +2.5V.

The AD780 2.5V reference is used to supply the +2.5V bias voltage to the AD712s as well as provide an external reference to the AD776. While the AD776 internal reference is adequate for most applications (simply connect REFOUT to REFIN), power supply rejection and overall regulation may be improved by using an external reference such as the AD780. In either case, the REFIN pin should be bypassed to a low-impedance ground plane with a 100μF capacitor to absorb the transients produced by the internal switched capacitors.

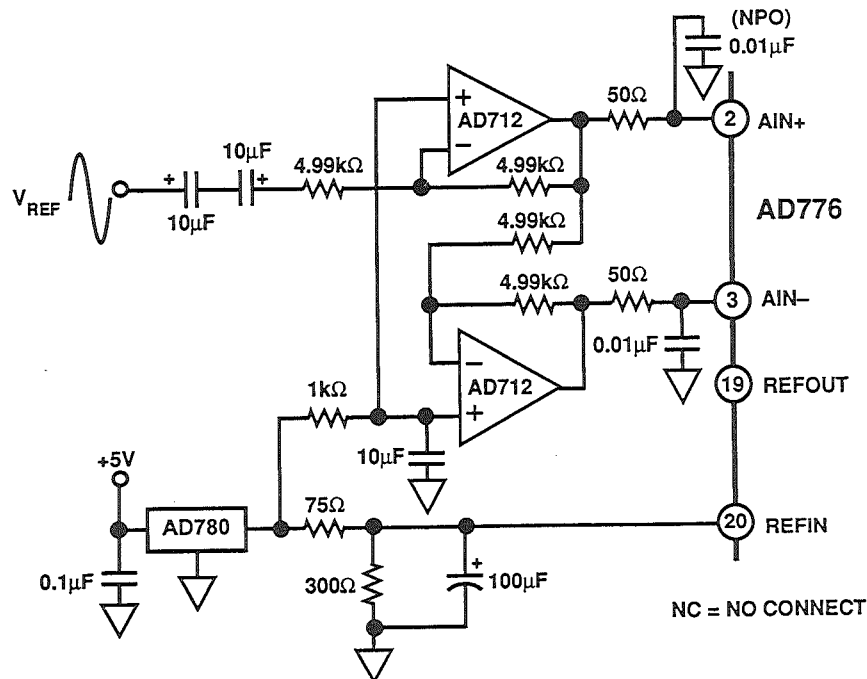## SINGLE-ENDED TO DIFFERENTIAL DRIVE CIRCUIT FOR THE AD776 SIGMA-DELTA ADC

Figure 14.25

14

DESCRIPTION OF AD1879 18 BIT SIGMA-DELTA AUDIO ADC

The AD1879 is a dual 18 bit sigma-delta ADC designed for professional digital audio. A block diagram of the device is shown in Figure 14.26, and performance specifications are given in Figure 14.27. The modulator is a fifth-order switched capacitor design which shapes the noise spectrum as shown in Figure 14.28. The oversampling ratio is 64x, which places the oversampling frequency at 3.072MHz for the standard audio sampling rate of 48kHz. Because of the high oversampling ratio, a single-pole analog antialiasing filter is sufficient at the input of the ADC.

For audio ADCs such as the AD1879, the digital lowpass filter cannot be implemented using standard multiply-accumulate structures. For example, we require a filter which operates at a sample rate of 3.072MHz (64 x 48kHz),

is flat to 20kHz and has a stopband attenuation of over 115dB starting at 26.2kHz. If we evaluate these requirements in a standard FIR equiripple design program, the number of coefficients required is 4096. At an output sample rate of 48kHz, we would require a multiply-accumulate time of 5.1ns. This is too fast for a standard FIR filter structure to implement because of semiconductor process limitations. For this reason, we must use either a parallel processing approach where more than one multiply-accumulate is being executed at any one time, or a multi-rate approach where the decimation is done in more than one step. For the AD1879, a parallel processing approach was chosen (Reference 1). The characteristics of this filter are given in Figure 14.29, and the amplitude response in Figure 14.30.
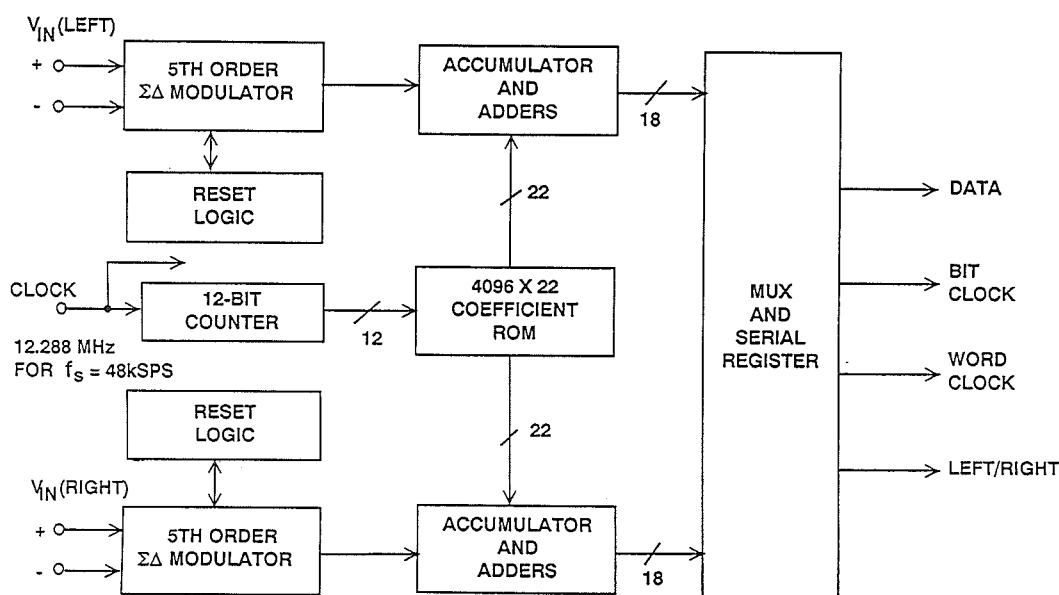
AD1879 DUAL 18-BIT SIGMA-DELTA ADC

Figure 14.26

AD1879 18 BIT SIGMA-DELTA ADC KEY SPECIFICATIONS

- ■ Two 18 Bit Channels for Stereo Digital Audio

- ■ Interchannel Crosstalk: -105dB at 1kHz

- ■ SNR: 103dB

- ■ THD + N: 98dB

- ■ Oversampling Ratio: 64x

- ■ Output Word Rate: 55kHz Maximum

- ■ Linear Phase Digital Filter

- ■ Power: 900mW

- ■ 28 Pin, 600-mil Plastic Package

Figure 14.27

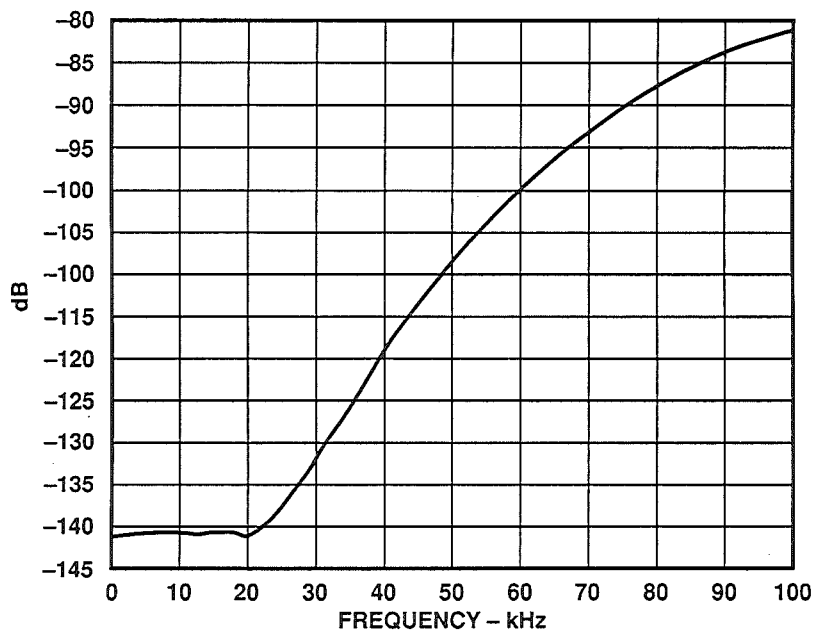# AD1879 NOISE SHAPING FUNCTION

Figure 14.28

AD1879 DIGITAL FILTER CHARACTERISTICS

- ■ Stopband Attenuation: 118dB

- ■ Passband Ripple: 0.0004dB

- ■ Cutoff Frequency (48kHz output rate): 21.7kHz

- ■ Stopband Frequency (48kHz output rate): 26.2kHz

- ■ Number of Parallel Accumulators: 64 27-bit accumulators

- ■ Coefficient Wordlength: 22bits

- ■ Equivalent Number of Taps: 4096
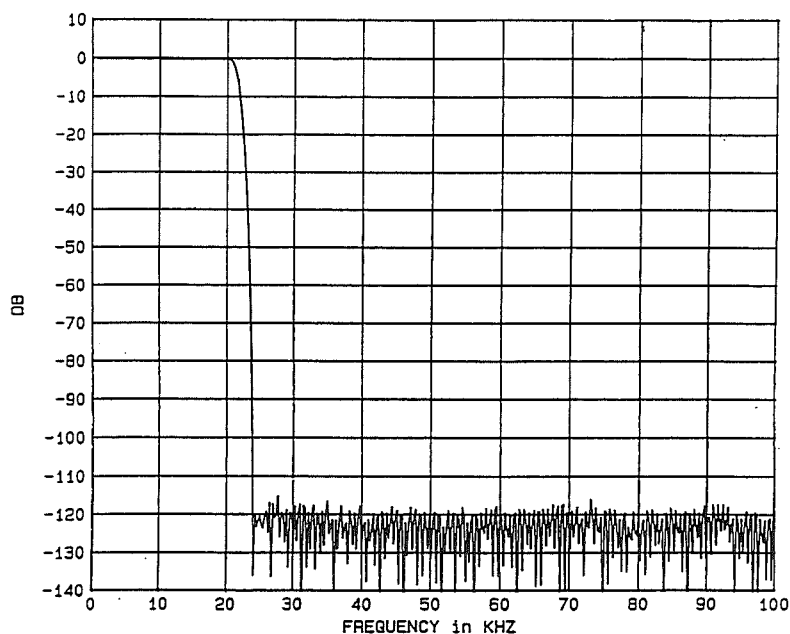
Figure 14.29

AD1879 DIGITAL FILTER RESPONSE

Figure 14.30

The AD1879 ADC is a compound monolithic IC. This means that the package contains two monolithic chips but no other components. One chip performs the sigma-delta modulation function, while the second chip performs the digital filtering.

The sigma-delta modulator in the AD1879 is fully differential and each channel has the equivalent input circuit shown in Figure 14.31. For optimum common mode rejection of transient load currents, the input should be driven differentially. The differentially connected $0.0047\mu F$ capacitor supplies most of the differential-mode transient currents, while the $0.01\mu F$ capacitors connected to ground absorb spike currents which are common mode. The 51Ω series resistors isolate the remaining transient current from the drive amplifiers as well as isolating the capacitive loads from the op amp outputs. These resistors must be small, however, in order to avoid distortion from the signal-dependent transients caused by charge injection. The OP-275 (dual) op amp is recommended as a precision low-distortion drive amplifier.

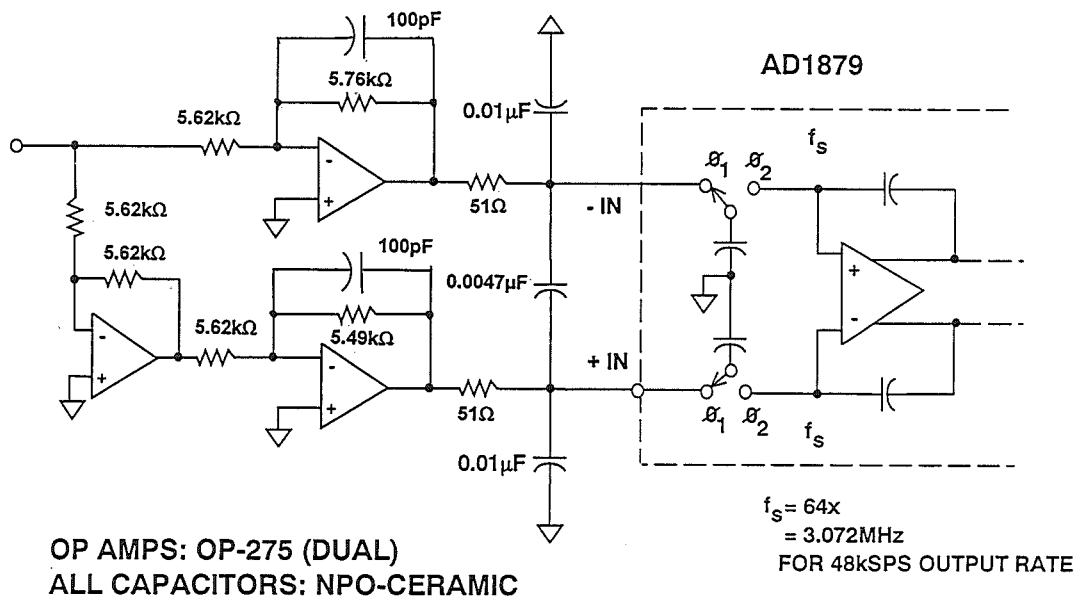## DIFFERENTIAL DRIVER (ONE CHANNEL)
FOR THE AD1879 SIGMA-DELTA AUDIO ADC

Figure 14.31

SIGMA-DELTA DACs

Sigma-delta D/A conversion can generally be thought of as the A/D conversion process in the reverse order, where all the basic functions of the digital filter and sigma-delta modulator previously discussed are the same. Sigma-delta DACs offer essentially the same advantages as sigma-delta ADCs. Because of the large oversampling ratio, the requirements on the antialiasing reconstruction filter are greatly relaxed. However, care must be taken to make sure the high frequency noise components contained in the one-bit DAC output are filtered sufficiently. If a higher order filter is required to reduce this noise, then some of the advantages of the sigma-delta DAC architecture are lost.

Accurate, low-cost, high resolution laser wafer trimmed DACs are readily available, and for this reason there has been little pressure to fully exploit sigma-delta DACs at the component level. The incentive for developing the sigma-delta DAC technology is because it is ideal for mixed-signal ICs which require the chip-level integration of ADC, DAC, and DSP functions.

SIGMA-DELTA DAC CONCEPTS

■ Basically a Sigma-Delta ADC in Reverse

■ Low-Cost, High Resolution R/2R DACs with Oversampling Capability Already Exist

■ Sigma-Delta DACs Ideal for Chip-Level Integration with ADC and DSP Functions

■ Antialiasing Filter Must Remove High Frequency Noise

Figure 14.32

The traditional approach to achieving high performance and wide dynamic range using R/2R-based DACs is shown in Figure 14.33. Due to the binary nature of the internal DAC switches, code-dependent transients, or glitches, typically produce some amount of non-filterable in-band harmonic distortion in the output spectrum. As discussed previously in the DAC section of this seminar, a technique called segmentation can greatly minimize these effects. For the ultimate in spectral purity, the remaining glitches can be removed with a sample-and-hold circuit which isolates the DAC output voltage for the duration of the glitch. This technique can eliminate the code-dependent glitches (hence harmonic distortion) at the expense of introducing some additional energy at the sampling frequency, which is filterable. A lowpass, or smoothing filter is required at the output of the SHA to prevent aliasing as well as eliminate the energy at the sampling rate. The same basic considerations used to define the antialiasing filter used ahead of an ADC apply to the smoothing filter which follows the DAC. For this reason, oversampling relaxes the smoothing filter rolloff requirements in a similar manner. In fact, 2×, 4×, and 8× oversampling techniques are currently in widespread use in compact disk players which use conventional R/2R 16, 18, and 20 bit DACs.

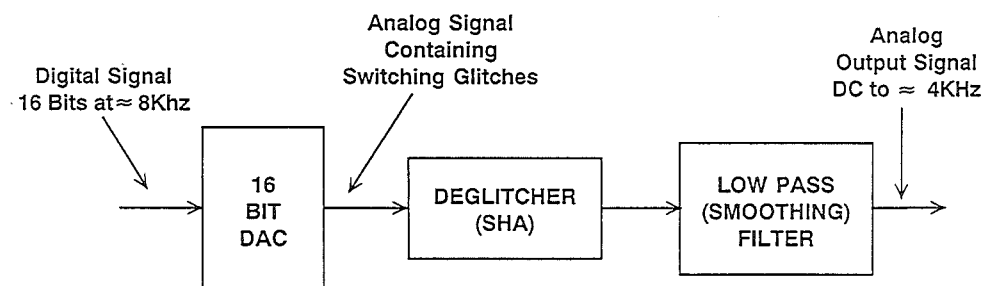## CONVENTIONAL DAC DEGLITCHING USING A SHA

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Figure 14.33

The main elements used to implement a sigma-delta DAC are shown in Figure 14.34. The example shown here is for a 16 bit DAC which is updated at an 8kHz rate to produce a voiceband output signal having a bandwidth of 4kHz. The 16 bit digital word is fed to a digital interpolation filter where the sampling rate is increased to 1.024MHz, corresponding to an oversampling ratio of 128. This process can be viewed as the reconstruction of a new, higher rate digital signal from an older, lower rate digital signal. Figure 14.35 shows the interpolation of a discrete time signal by a factor of 4. The input signal x(m) is expanded by inserting three zero-valued samples between

data samples. The resulting signal w(m) is lowpass filtered to produce y(m) whose sample rate is increased by a factor of 4. This process may be thought of as *undecimation*.

The digital-input sigma-delta modulator noise-shapes the 16-bit 1.024MHz data stream and reduces the sample width to one bit. Unlike the sigma-delta modulator in a sigma-delta ADC, this modulator is all digital. The transfer function is implemented in the digital domain with an IIR filter. This digital filter performs the same modulator function as in the ADC, where the input signal is effectively lowpass filtered, and the quantization noise is high-pass filtered.

SIGMA-DELTA DAC

Filter Output
16 Bits at≈ 1 MHz

Modulator Output
1 Bit at≈ 1 MHz

Analog
Output Signal
DC to ≈ 4KHz

| INTERPOLATION FILTER | SIGMA DELTA MODULATOR | 1 BIT D/A | OUTPUT FILTER |

DIGITAL

DIGITAL

Digital Signal
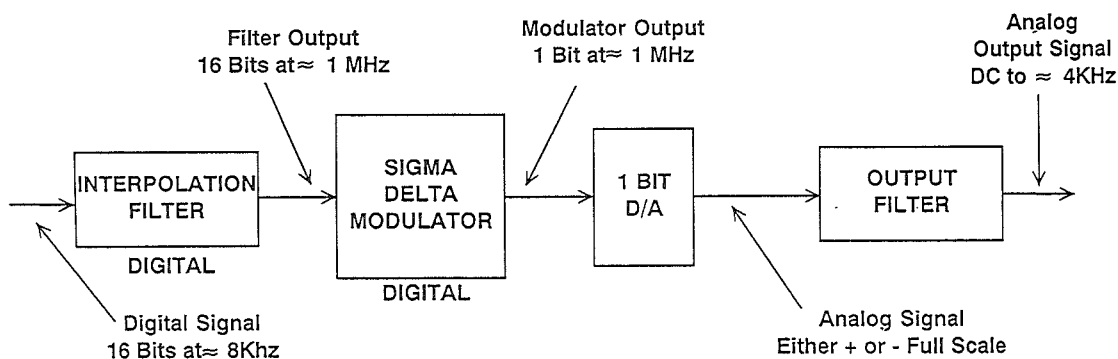16 Bits at≈ 8Khz

Analog Signal
Either + or - Full Scale

Figure 14.34

As in the case of a sigma-delta ADC, the 1 bit DAC output is useless until it is averaged in some manner. Also, there is a need to remove the shaped quantization noise present in the upper frequency area. There is also a need to reject any images above the output Nyquist rate. The analog smoothing filter performs these functions, usually in several stages. It is important for the design of this filter that the filter characteristics match the requirements of the overall system. For example, an audio system would need to have its phase and amplitude response preserved while the output filter also provides the appropriate rejection of higher frequency components. If the smoothing filter is an active filter, care must be taken that the op amps used do not introduce distortion products in the final output due to slewrate limiting and noise.

INTERPOLATION OF A DISCRETE-TIME SIGNAL

INPUT SIGNAL   x(m)

ADDED ZERO SAMPLES   w(m)

FILTERED OUTPUT SIGNAL (Sampling Rate is Increased)   y(m)
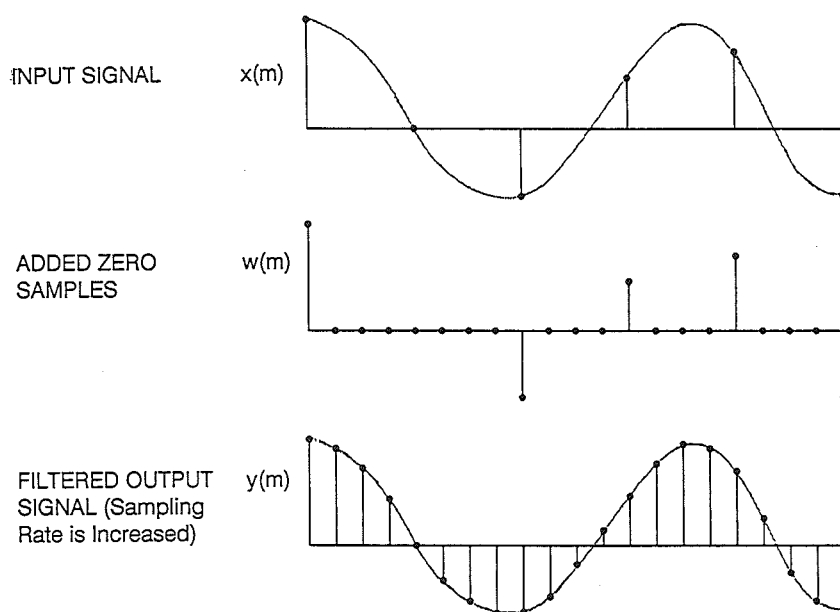
Figure 14.35

THE AD28MSP02 SIGMA-DELTA CODEC

The AD28msp02 is a mixed-signal peripheral device available based on sigma-delta design. The device is a linear codec with a 16-bit sigma-delta ADC and DAC, thereby providing a complete analog front end and back end for high performance voiceband DSP applications. Key features of the IC are summarized in Figure 14.36 and a functional block diagram is shown in Figure 14.37.

KEY FEATURES OF THE
AD28msp02 SIGMA-DELTA CODEC

■ 16 bit Sigma-Delta ADC

■ 16 bit Sigma-Delta DAC

■ On-Chip Antialiasing and Smoothing Filters

■ 8kSPS Sampling Rate, 128x Oversampling Ratio

■ On-Chip Voltage Reference

■ 65dB SNR and THD

■ Easy Interface to DSP Chips

■ 24-pin DIP/SOIC Package

■ Single +5V Supply, 100mW Power Dissipation

■ Ideal for Voiceband Applications
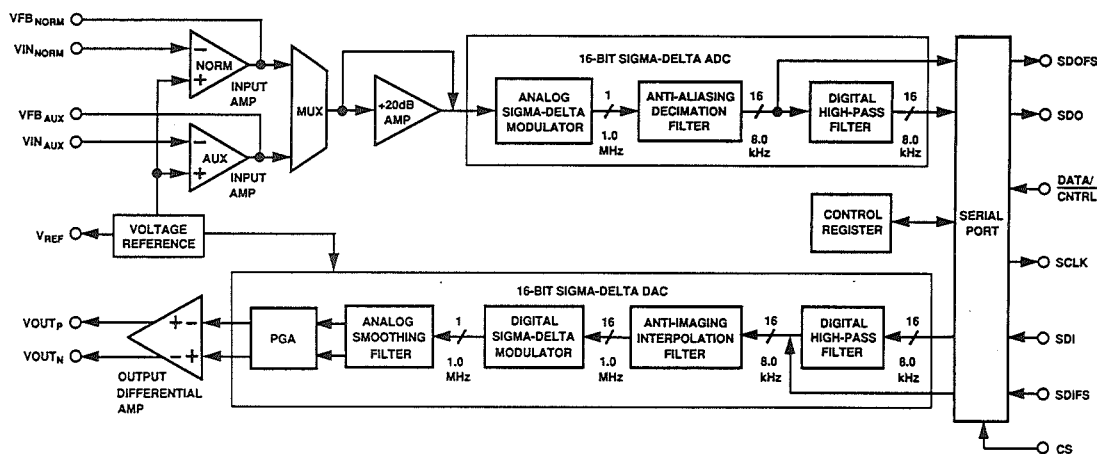
Figure 14.36

AD28msp02 VOICEBAND SIGMA-DELTA CODEC

Figure 14.37

Compared to traditional μ-law and A-law codecs, the AD28msp02's linear coded ADC and DAC maintain wide dynamic range throughout the transfer function. An effective sampling rate of 8kSPS coupled with 65dB SNR and THD performance make the device attractive in many telecommunications applications such as digital cellular telephones. The part is packaged in a 24-pin DIP/SOIC package ensuring a highly integrated and compact solution to voiceband analog processing requirements. The AD28msp02 easily interfaces to the ADSP-2101, ADSP-2105, ADSP-2111, MC56001 and TMS320C25 DSP processors via its serial I/O port (SPORT).

The encoder side of the AD28msp02 consists of two selectable analog input amplifiers and a sigma-delta ADC. The gain of the input amplifiers can be adjusted with the use of external resistors from -12dB to +26dB. An optional 20dB preamplifier can be inserted before the modulator. The preamplifier and the multiplexer are configured by bits in the control register. The sigma-delta ADC consists of a sigma-delta modulator, an antialiasing decimation filter, and a digital high pass filter. The modulator noise-shapes the signal and produces 1-bit samples at 1.024MHz. This bit stream, representing the analog input, is fed to an antialiasing decimation filter which consists of two lowpass filter stages. The first stage reduces the sampling rate to 40kHz and increases the sample width to 16 bits; the second further reduces the sampling rate to 8kSPS. Each resulting sample is then loaded into the SPORT for transmission.

The decoder consists of a sigma-delta DAC and a differential output amplifier. The DAC reads 16-bit samples at an 8kHz rate from the SPORT. The samples are low- and high-pass filtered by the digital anti-imaging and high pass filters. The anti-imaging filter interpolates the sampling rate in two stages, first to 40kHz, and then to 1.024MHz. The resulting 16-bit samples are processed by the digital sigma-delta modulator which reduces the sample width to 1 bit. This bit stream is fed to an analog smoothing filter which converts the data to an analog voltage. The gain of the smoothing filter can be adjusted via the control register from -15dB to +6dB is 3dB steps.

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MULTISTAGE NOISE SHAPING (MASH) SIGMA-DELTA CONVERTERS

Non-linear stabilization techniques have been successfully used to design a fifth-order sigma-delta loop in the AD1879 audio ADC. An alternative approach, called multistage noise shaping (MASH) utilizes cascaded stable first-order loops. Figure 14.38 shows a block diagram of a three-stage MASH ADC. The output of the first integrator is subtracted from the first DAC output to yield the first stage quantization noise, Q1. Q1 is then quantized by the second stage. The output of the second integrator is subtracted from the second DAC output to yield the second stage quantization noise which is in turn quantized by the third stage.
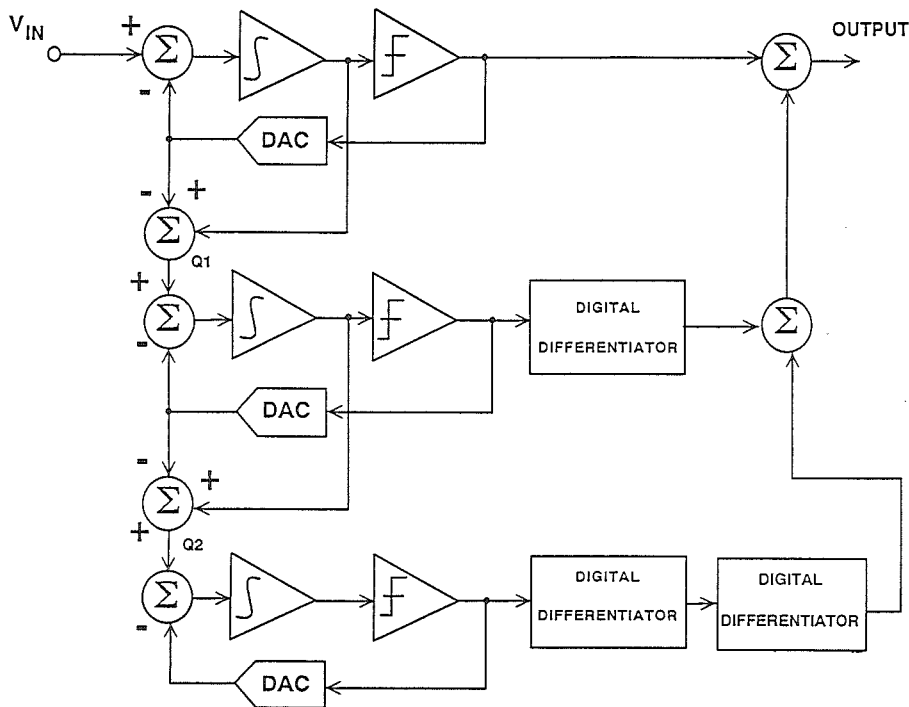
MULTI-STAGE NOISE SHAPING SIGMA-DELTA ADC (MASH)

Figure 14.38

MASH TOPOLOGY VERSUS
HIGHER-ORDER LOOP SIGMA-DELTA CONVERTERS

■ MASH Cascades Single-Order Loops, therefore Easy to Stabilize

■ Gain and Phase Matching Critical in MASH Converters for Errors
to Cancel

■ MASH Digital Differentiators Must Match Analog Integrators

■ Single-Loop Higher Order Modulators Less Subject to Idling
Patterns

■ Single-Loop Higher Order Modulators More Difficult to Understand,
Analyze, and Stabilize, But Can Be Done Using Non-Linear
Techniques as in AD1879 (5th Order Modulator)

Figure 14.39

The output of the first stage is summed with a single digital differentiation of the second stage output and a double differentiation of the third stage output to yield the final output. The result is that the quantization noise Q1 is suppressed by the second stage, and the quantization noise Q2 is suppressed by the third stage yielding the same suppression as a third-order loop. Since this result is obtained using three first-order loops, stable operation is assured. A comparison of the MASH architecture with the higher-order single-loop architecture is given in Figure 14.39.

MULTI-BIT SIGMA-DELTA CONVERTERS

So far we have considered only sigma-delta converters which contain a single-bit ADC (comparator) and a single-bit DAC (switch). The block diagram of Figure 14.40 shows a multi-bit sigma-delta ADC which uses an n-bit flash ADC and an n-bit DAC. Obviously, this architecture will give a higher dynamic range for a given oversampling ratio and order of loop filter. Stabilization is easier, since second-order and higher loops can be used. Idling patterns tend to be more random thereby minimizing tonal effects.
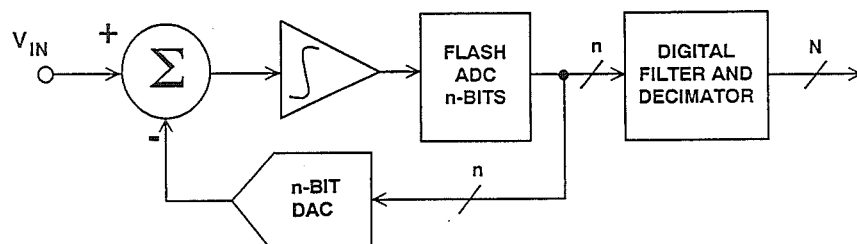
MULTI-BIT FIRST-ORDER SIGMA-DELTA ADC

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Figure 14.40

The real disadvantage of this technique is that the linearity depends on the DAC linearity, and thin film laser trimming is required to approach 16-bit performance levels. This makes the multi-bit architecture extremely impractical to implement on mixed-signal ICs. A comparison of the multi-bit versus single-bit sigma-delta converter is given in Figure 14.41.

MULTI-BIT VERSUS SINGLE-BIT SIGMA-DELTA CONVERTERS

Multi-Bit: ■   Higher Dynamic Range for Given Oversampling Ratio and Loop Filter Order

    ■   Higher Order Systems Easier to Stabilize

    ■   Fewer Tonal Effects due to Idling Patterns

    ■   Linearity Depends on DAC

    ■   Thin Film Laser Trimming Required

Single-Bit: ■   Perfect Linearity, no Strict Matching Requirements

    ■   No Laser Trimming Required

    ■   Perfect Topology for Mixed-Signal VLSI

    ■   Non-Linear Techniques Required to Stabilize Higher Order Loops (AD1879)

Figure 14.41

SIGMA-DELTA SUMMARY

Although the concepts used in sigma-delta converters are not new by any means, their recent proliferation has been primarily driven by the need for converters which are compatible with mixed-signal VLSI chips. The sigma-delta architecture is ideal for converters for measurement, voiceband, and audio applications. Further exploration of various sigma-delta circuit topologies combined with the development of new processes is sure to push the maximum dynamic range and sampling rates even higher.

It is clear that the sigma-delta converter is not the answer to all data acquisition requirements at the present time. Upper sampling frequency is limited, thereby excluding video applications, fast multiplexing of inputs is difficult due to the settling time of the internal digital filter, and out-of-range signals may cause saturation of the internal modulators.

On the other hand, the inherently good performance without the need for laser trimming, the relaxation of antialiasing and anti-imaging filter requirements due to oversampling, and the basic sampling nature of the architecture without the need for a SHA will keep sigma-delta development moving at a rapid pace as mixed-signal ICs proliferate.

SIGMA-DELTA SUMMARY

■ Inherently Excellent Linearity

■ Ideal for Mixed-Signal IC Processes, no Trimming

■ No SHA Required

■ Upper Sampling Rate Currently Limits Applications to Measurement, Voiceband, and Audio - But Bandpass Sigma-Delta Techniques Will Change This

■ Out-of-Range Signals May Cause Modulator Saturation

■ Analog Multiplexing Applications Limited by Internal Filter: Use one Sigma-Delta ADC per Channel!

Figure 14.42

14

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